CLAIMS

What is claimed is:

1. A silicon-on-insulator transistor comprising:
an insulating layer;
an active region overlying the insulating layer, the active region comprising:
an intrinsic body region;
a body tie access region also overlying the insulating layer and laterally adjacent the intrinsic body region, the body tie access region making electrical contact to the intrinsic body region; and
a body tie diffusion laterally offset from the body tie access region and electrically coupled to the body tie access region;
a gate electrode overlying the intrinsic body region for providing electrical control of the intrinsic body region of the silicon-on-insulator transistor and extending over a portion of the body tie access region; and
first and second current electrodes adjacent opposite sides of the intrinsic body region.

2. The silicon-on-insulator transistor of claim 1 further comprising:
a dielectric layer overlying substantially all of the body tie access region including the portion of the gate electrode that overlies the body tie access region.

3. The silicon-on-insulator transistor of claim 2 wherein the dielectric layer functions as a sidewall spacer of the gate electrode.

4. The silicon-on-insulator transistor of claim 2 wherein a portion of the body tie access region that underlies the dielectric layer comprises doped material that increases doping concentration of the body tie access region to substantially minimize formation of a depletion region in the body tie access region.

5. The silicon-on-insulator transistor of claim 4 wherein doping of the portion of the body tie access region is provided by using a pattern feature in a first mask and reusing the pattern feature in a second mask to provide the dielectric layer.

6. The silicon-on-insulator transistor of claim 1 wherein the gate electrode does not extend over more than one-half of the body tie access region to minimize parasitic gate capacitance and current leakage.

7. A method for forming a silicon-on-insulator transistor comprising:

providing an insulating layer;

forming an active region overlying the insulating layer, a portion of the active region providing an intrinsic body region;

forming a body tie access region within the active region and also overlying the insulating layer and laterally adjacent the intrinsic body region, the body tie access region making electrical contact to the intrinsic body region;

forming a gate electrode overlying the intrinsic body region for providing electrical control of the intrinsic body region of the silicon-on-insulator transistor and extending over a portion of the body tie access region to minimize parasitic capacitance and gate electrode leakage;

forming first and second current electrodes adjacent opposite sides of the intrinsic body region; and

forming a body tie diffusion within the active region and laterally offset from the body tie access region and electrically coupled to the body tie access region.

8. The method of claim 7 further comprising:

forming a dielectric layer overlying substantially all of the body tie access region including the portion of the gate electrode that overlies the body tie access region.

9. The method of claim 8 further comprising:

doping a portion of the body tie access region that underlies the dielectric layer to increase doping concentration of the body tie access region to substantially minimize formation of a depletion region in the body tie access region.

10. The method of claim 9 wherein the doping further comprises:

using a pattern feature in a first mask as a first selective block for the doping; and

reusing the pattern feature in a second mask as a second selective block to provide the dielectric layer.

11. The method of claim 7 further comprising:

minimizing parasitic gate capacitance and current leakage by not extending the gate electrode over more than one-half of the body tie access region.

12. A method of forming a silicon-on-insulator transistor comprising:

forming an insulating substrate;

defining an active region which defines a location of the silicon-on-insulator transistor;

implanting the active region with a predetermined diffusion material to form an intrinsic body region of desired doping concentration;

defining a body tie access region by forming an opening in a mask overlying the active region;

implanting the active region to form the body tie access region, the body tie access region having a predetermined doping concentration to minimize body tie access resistance;

forming a gate oxide overlying both the intrinsic body region and the body tie access region;

depositing and patterning a substantially constant length gate electrode material overlying the intrinsic body region and a portion of the body tie access region;

forming halo/extension implants of dopants into the intrinsic body region while substantially blocking the halo/extension implants of dopants from the body tie access region;

forming sidewall spacer dielectric material overlying the substantially constant length gate electrode material and body tie access region;

masking a region substantially overlying the body tie access region using a mask;

removing the sidewall spacer dielectric material substantially everywhere except overlying the body tie access region and adjacent the substantially constant length gate electrode material;

forming a source diffusion region and a drain diffusion region; and

forming a body tie diffusion region.

13. The method of claim 12 further comprising:
forming electrical contact to the source diffusion region, the drain diffusion region, the body tie diffusion and the substantially constant length gate electrode material by forming a silicide layer overlying the source diffusion region, the drain diffusion region, the body tie diffusion and the substantially constant length gate electrode material.

14. The method of claim 12 further comprising:
defining a dimension of the mask used for masking the body tie access region to have a minimum distance necessary to prevent dopants implanted into the source diffusion region and the drain diffusion region from also being implanted into the body tie diffusion and vice versa.

15. The method of claim 12 further comprising:
depositing and forming a conductive material selectively overlying each of the source diffusion region, the drain diffusion region, the substantially constant length gate electrode material and the body tie diffusion region for making electrical contact thereto.

16. The method of claim 15 further comprising:
defining a dimension of the mask to have a value substantially large enough to prevent electrical short circuiting by the silicide contacting each of the source diffusion region, the drain diffusion region, the body tie diffusion region and the substantially constant length gate electrode material.

17. The method of claim 12 further comprising:
forming the gate oxide overlying the body tie access region to have a first thickness that is greater than a second thickness of the gate oxide overlying the intrinsic body region by using the mask.

18. The method of claim 12 further comprising:
extending the substantially constant length gate electrode material to overlie less than one-half of the body tie access region.